MEMORY SYSTEM OF THE COMPUTER SANK-1

A pioneer work late 1950s

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Abstract

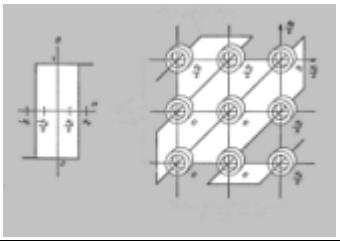
New electronic components as transistors and ferrite cores made it possible to start the building of small and fast computers during the second half of 1950s. The Swedish aircraft company, SAAB AB, finished SANK-1, a prototype computer, during 1960 and demonstrated its use both for military and commercial applications (see note).
One important part of the computer, the memory system, was an advanced design effort at that time. The work included the selection of transistor types and the design and testing of reliable transistor circuits to write and read information in the ferrite core memory.

Key words

Computer, SANK-1, memory system, transistor circuits.

Note. The computer is well preserved and is exhibited in the historical computer museum **IT-ceum** at Mjärdevi Science Park in Linköping, Sweden.

In 1953 a new computer memory was tested in the Whirlwind computer at MIT. The memory element was a small toroid of a ferromagnetic material with a square shaped magnetic hysteresis loop. Magnetic flux in one direction was defined as a binary "1" and in opposite direction as a binary "0". The new memory was a true random access memory, it was fast, and above all, it was reliable. It became the dominant fast memory in computers for the next decade.



1. A ferrite core memory with transistor circuits

At the end of 1950s ferrite cores became available in quantities and with good quality. They also became smaller, which made the ring formed cores, around 1 millimetre in size, useful for transistor circuits. It was a technical challenge to design and build a coincident current memory system to demonstrate its use in a computer. It involved the need to find the best operating condition for the ferrite cores and to build a memory package with over 20.000 small cores. There was also a need to find transistors to switch the cores, to design circuits for temperature and voltage variations and to get an overall reliable operation. Many engineers were involved in the design and building of the prototype computer SANK-1, SANK/D2 or Saab D2 as it was named later on. SAAB AB in Linköping (ref.1, p 15), finished the computer in 1960, figure 1. SANK-1 was part of a study by the Swedish Air Force to learn if a digital computer could be used in a combat aircraft. The memory system, as described below, was the base for memories in the airborne computer CK37 for aircraft Saab 37 Viggen and the Saab D21 series for commercial applications.

Figure 1. The prototype computer SANK-1 or SaabD2 with strip reader, punch, digital display and the operator. In operation from October 1960

2. Ferrite cores

Late 1958, a batch of ferrite cores was delivered to Saab. Careful testing started to find the best operating conditions. A special tester was built to switch the cores (reversing of the magnetic flux) by a specific current pulse. Safe operation of a coincident core memory requires knowledge of switching current size and shape and output voltage representing “1” or “0”. Necessary to know is also core characteristics at different temperatures. The marginal design was carried through for one type of ferrite core (ref. 2). The selected core, 1,2 mm S4M-F-764 from Plessey in England, required a constant drive current of 362 mA at a voltage of 20 volt, within 25–47 °C. Another operating alternative was to compensate the current versus temperature, -1,6 mA/°C from 25 to 66°C.

The following description of the memory system is a shorted summary and translation from a technical design description (ref. 3). Some of the figures are copied from this reference.

3. The memory packet

A memory packet of 1024 words with 20 bits was designed and fabricated at Saab. It was made of 20 matrices, each arranged with 32x32 cores, figure 3. Each core in the matrices, oriented according to the figure, is sewed with 4 thin copper wires, x- and y-wire (rows and column), and information read-out wire and inhibit wire. The x- and y- wires are soldered at the four sides to soldering pins, separated by isolation washers which together form a frame around the cores. The read and inhibit wires are soldered to pins at each corner. An isolating laminate is glued to the core matrix and gives the whole plane a resonant frequency of 750 Hz. The 20 matrices are connected together by joining the soldering pins to form a complete memory packet, figure 2. Outgoing connections are available on a separate coupling board. A µ-metal screen, to avoid external disturbances, encloses the whole packet. In addition the computer has another memory of 256 twenty bit words that stores variable data. Both memory systems have similar transistor circuits that are described below.

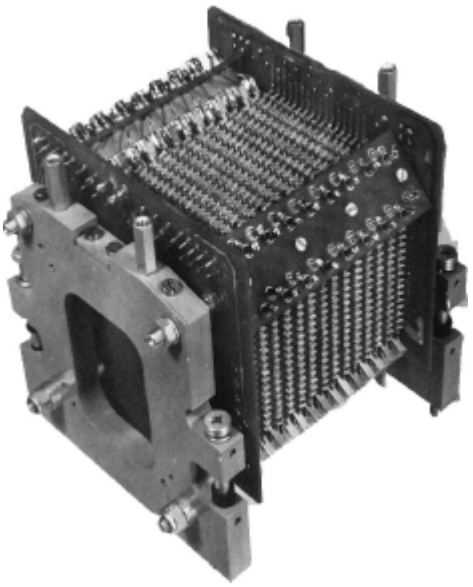


Figure 2. A complete memory packet of 1024 words without the µ-metal screen.

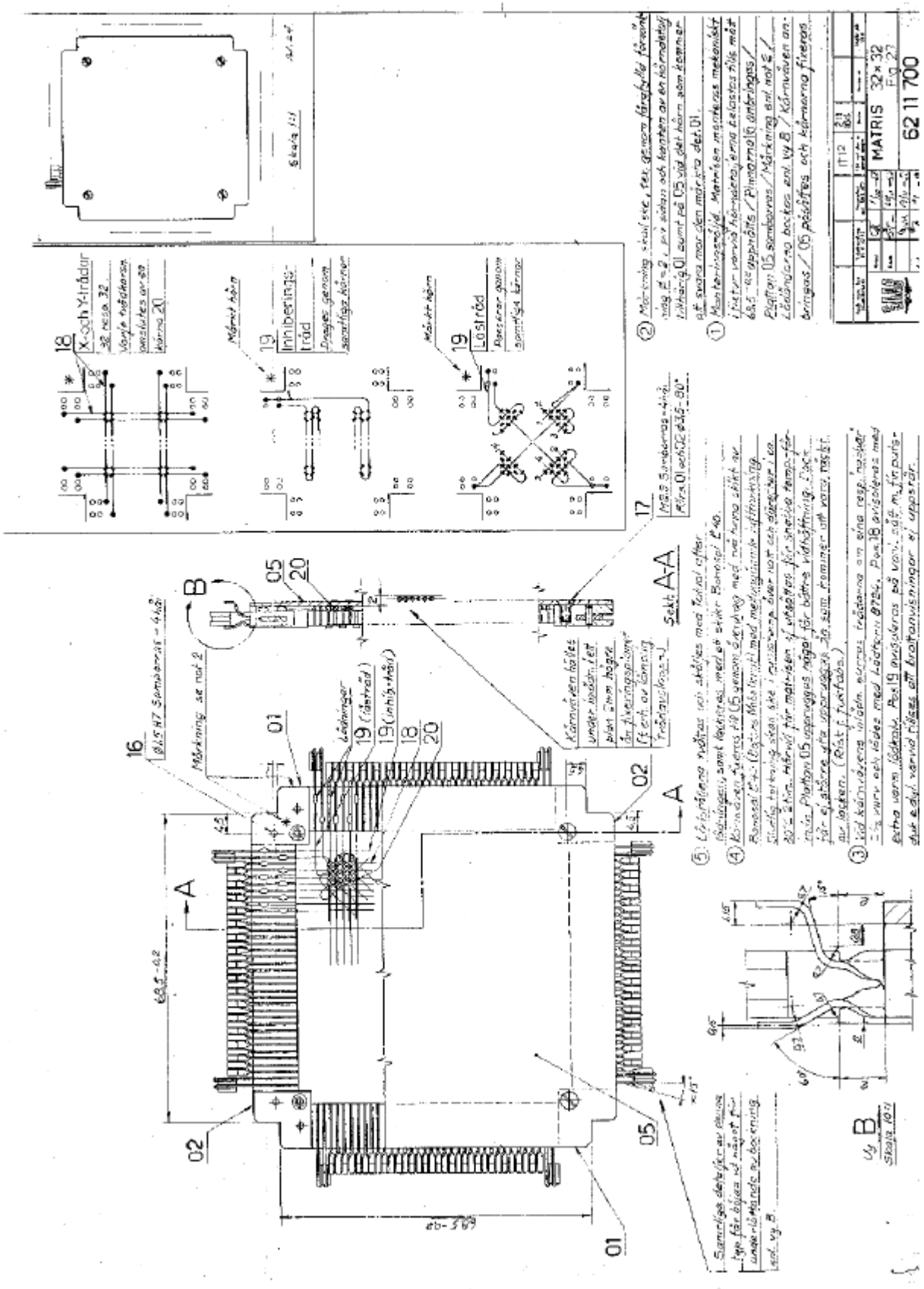


Figure 3. Part of drawing Saab 6211 700 showing the matrix design. 1/10 1958, signed by Ingvar Freijd. The drawing gives instruction of mechanical details with measures and how to thread the cores with four wires.

4. Memory system

The memory control unit, MCU, generates pulses that read or write information ”1” or “0” in selected cores. A full memory cycle is 5,6 microsec. This is a multiple, 14, of the computer clock pulses, 0,4 microsec. The control unit activates a circuit that generates an address pulse to select a word, a read and strobe pulse followed by a write and inhibit. The MCU is directed from the main controller in the central processor (ref. 4). The organisation of a coincident current memory system is shown in figure 4. All x- and y-wires (rows or columns) are coupled together at two terminals at one end of the matrix packet, MP. The terminals are connected to respective read or write current pulse drivers (DCR or DCC). These get information from the instruction memory register, IMR. At the other end is each of the x- and y-wires connected to individual address circuits (DR and DC) which are addressed from a word address register WAR. The address pulses occur simultaneously and last during the whole memory cycle until a new address is ordered. A new address is not allowed until 4 clock-pulses later when the address circuits have recovered.

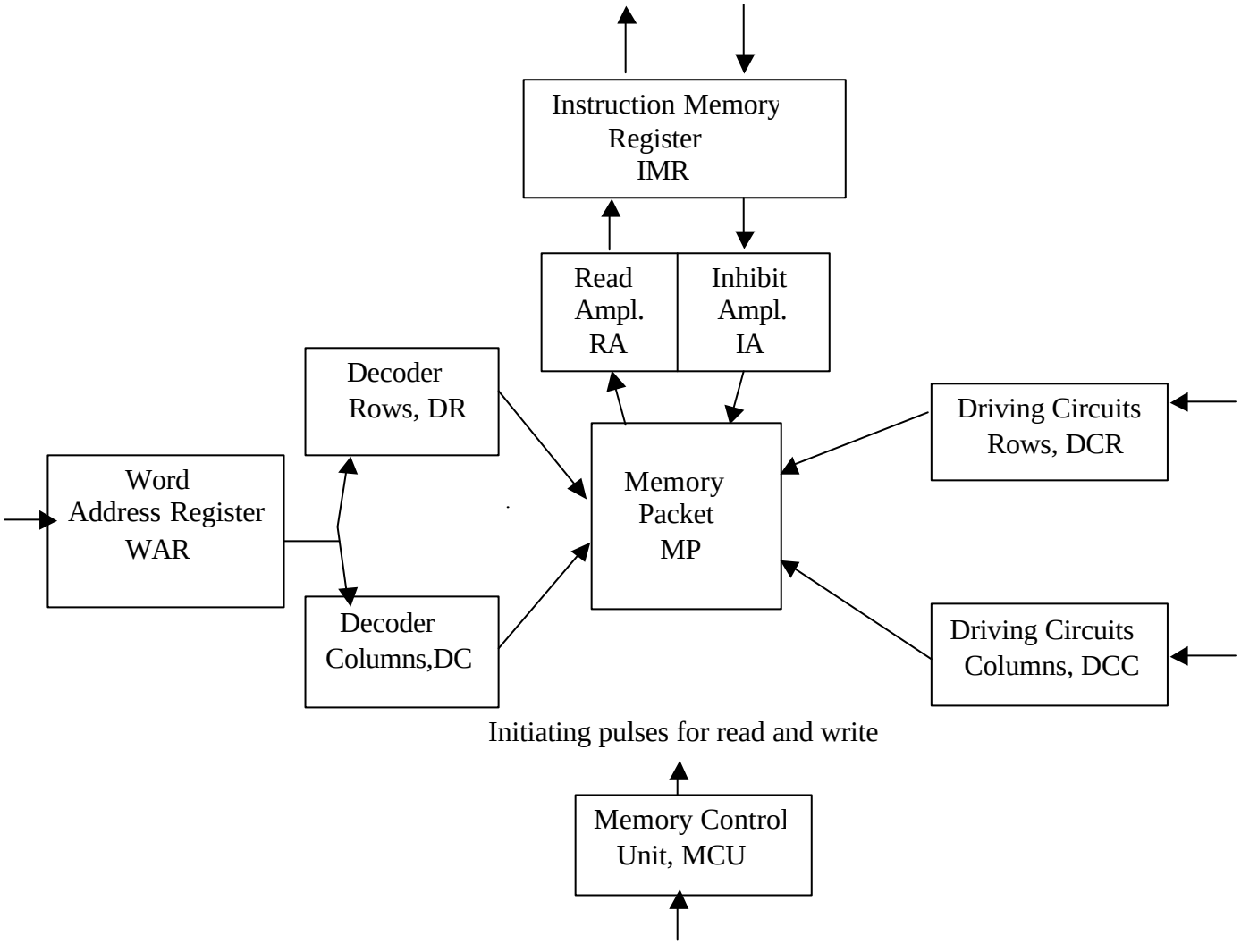


Figure 4. Organisation of a coincident current memory with communicating signals to and from the central processor

The register IMR is set at zero at the front of the address pulse. The half current read pulses through the x- and y- wires coincide to a full current read pulse in a selected word. This switches the magnetic flux in all word cores with “1”-information from “1” to “0”. Other

word cores along the x- and y-wires are only partly disturbed by the half current pulses. The read-out wire from each core in the selected word picks up a “1”-voltage, superimposed by halfpulse disturbances, and amplifies (RA) the output voltage. This information, “1” or “0” is then transferred to the instruction memory register, IMR. This information is used during the write cycle to write back the original information in the cores. Current pulses of opposite polarity are driven through the x- and y-wires during the write part of the memory cycle. This switches all selected cores from “0” to “1”. Information from the instruction register also affects, at the same time, the inhibit amplifiers (IA) to generate inhibit pulses. This half current pulse of opposite polarity prevents a core in a selected word to change to “1” if the information should be “0”. The IMR content is then transferred to the central arithmetic unit.

5. Driving and addressing circuits

Circuits that generate the read and write currents through the x- and y-wires (rows or columns), are made as two separate circuits as the read and write currents are of opposite polarity. The half current pulses have each an amplitude of about 200 mA, which is 400 mA in all cores of a selected word. The read, write, and inhibit pulses in addressed wires have a length of about 2 microsec. with a rise and fall time of about 0,1 microsec. The driving transistors, of germanium alloy junction types (ref. 6), consist of two parallel-connected Tr10 and Tr11 (2N317A, pnp) respective Tr12 and Tr13 (2N358A, npn), figure 5. They are fed from the emitter followers Tr6-9 that produce, together with the peak capacitors, the required short rise- and fall time.

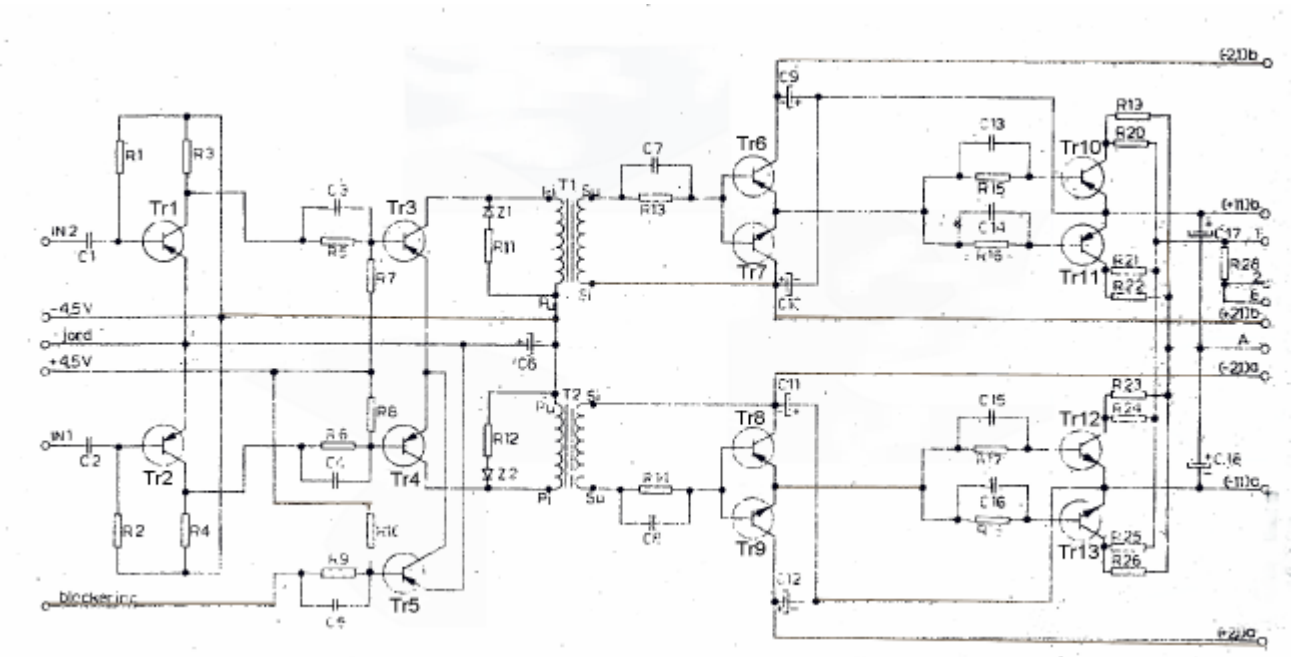


Figure 5. Read and write driving circuits according to Saab drawing 6212079.

The emitter followers are feed from transformer coupled circuits with transistors Tr3 and Tr4. Transformation is necessary to change the -4,5 voltage level to a higher level for the final driving transistors (about 11 volt). This higher level can also be changed when the driving pulse amplitude has to be altered with respect to working temperature of the ferrite cores.

The transistors Tr1 and Tr2 are feed with the initiating read and write pulses from the memory control unit. The circuits are RC-coupled to limit the output pulse to about 2,2 microsec. The time constant RC is 3630 nanosec. with selected components R=3,3 kohm ±1% and C=1100 pF ±1%. This controls the outgoing pulse length to always be 2,1–2,6 microsec within a range of –40 to +80° C. A blocking signal to Tr5 shuts off transistors Tr3 and Tr4 in order to prevent unintentional current pulses from destroying core information, e.g. at an uncontrolled current break.

The driving transistors dissipate power during operation. Available transistors, 2N317 and 2N358, could withstand about 150 milliwatt at +25° C. Dissipation power during operation includes power during max pulse current, leakage power when off and power at the rise and fall time of the current pulse. Power dissipation at pulse operation is difficult to calculate or measure. Junction temperature of the two transistor types was instead measured at continuous pulse operation on actual driving circuits (ref. 5). Pulse repetition rate was 6,4 microsec, collector current 115 mA at two environment temperatures 25 and 60° C. The transistors were attached to an AL heat sink, 60x80x10 mm. Totally 6 driving circuits were examined with 3 groups of specially measured transistors, “good”, “medium” and “less good”. The result at 60°C for 2N317 was a difference between junction temperature and environment temperature of about 7,5° C. For 2N358 it was about 14° because of a higher voltage drop and hence a higher dissipation during saturation, figure 6. Safe operation could thus be obtained at a junction temperature well below 75°C with selected “good” transistors.

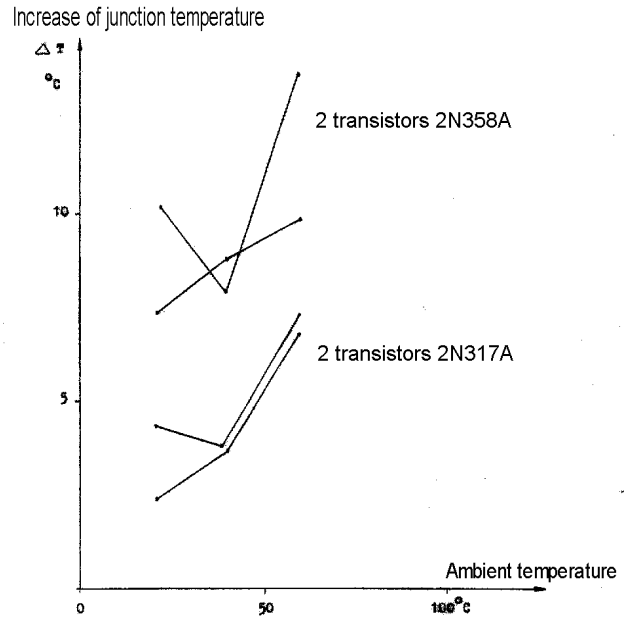


Figure 6. Increase of junction temperature above the ambient temperature at 25 and 60°C.

Another measurement was made to control the variation of rise and fall times versus different transistors and temperatures. Measurements showed that in the worst case the read pulse ended before the write pulse started, figure 7. The write pulse ended also before module number 15. The driving circuits were run for 5000 hours at 60°C to examine the long time effect. After this time the "good" transistors were still "good". The measurements resulted into use of specially selected "good" transistors in the driving circuits.

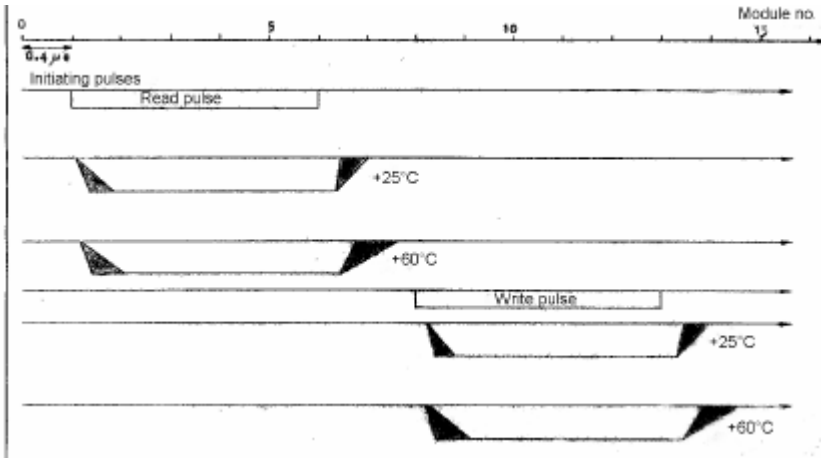


Figure 7. Variation of rise, recovery and fall times at 25 and 60°C. Shadowed areas shows the variation due to different transistors, "less good", "medium", "good".

The word address register, WAR in figure 4, has information to select a special word. Information is decoded by the address circuits DR and DC for each row and column (x- and y-wire). The circuits end with a special transistor for each of the 32 rows respective columns. This transistor is of a symmetric type, npn 2N569 (ref. 6). It can handle both read and write currents of opposite polarity, about 200 mA each. Medium dissipation during a memory cycle is about 25 mW with a junction temperature of 10°C above environment. Required base drive is about 8,5 mA. Circuits, including 2N595 and its drivers from the diode decoders, are specially selected in such a way that the recovery time of 2N595 is ended well before the next addressing at module number 19, figure 8.

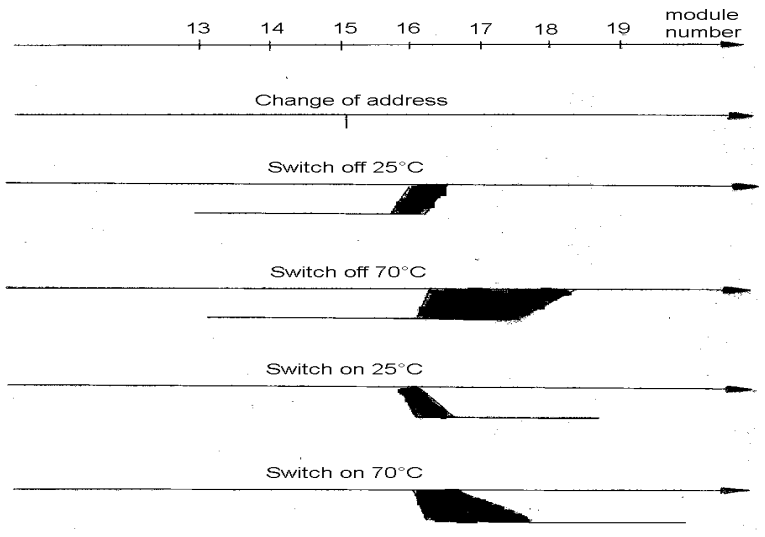


Figure 8. Time for recovery at address change at 20 and 70°C Shadowed areas shows how different transistors affects address change.

A negative voltage must block not selected address transistors. This voltage must exceed transients at current pulse rise and fall times. A transient voltage on a memory stack with 15 bits and 32x32 words was measured to about 5 volt at a rise time of the current pulse of about 0,1 microsec, figure 9. This voltage is added to the nominal collector potential –4,5 volt. -12 volt (with a safety margin) has been selected to reverse the base of all addressing transistors.

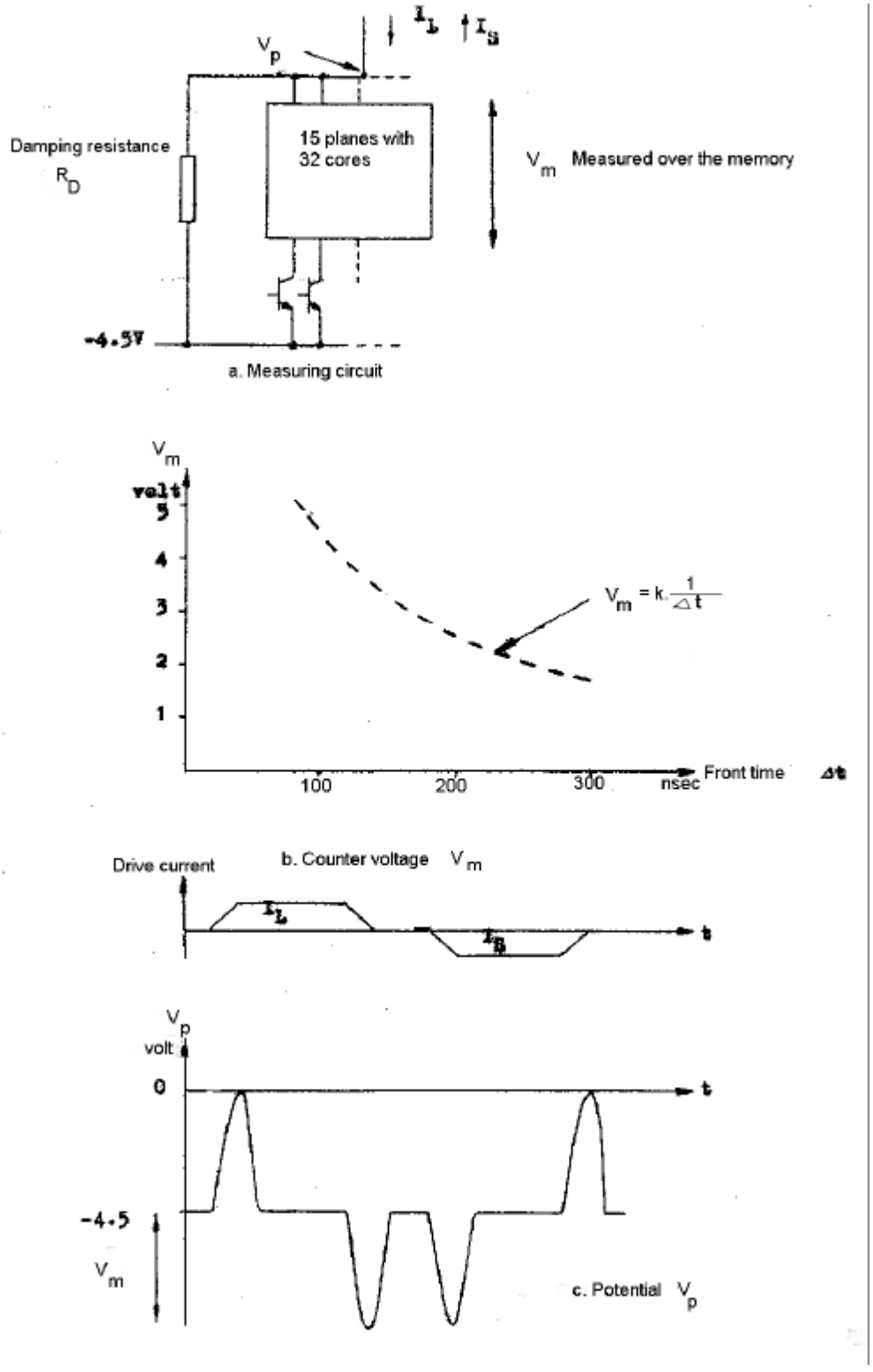


Figure 9. Transient's amplitude over a memory packet.

6. Read amplifiers

The amplifiers are designed to indicate “1” at more than 15 mV from the read wire. A “0” with max 10 mV output has to be suppressed. The read wire is also noisy from partly disturbed cores. According to figure 10 the read wire in the memory packet is connected over a damping resistor at the base of the amplifying transistor, Q1 2N393 (ref. 6). This works in class A with an amplification of about 230 times for average transistors at a collector current of 4 mA. The transformer (1:1:1) and the following transistors Q2 and Q3, 2N358 (ref. 6), rectify the amplified signals, positive or negative. The transistors are biased with 0,3 volt which results in a controlled amplitude discrimination. The transformer is loaded by two resistors, that reduce transients and gives the amplifying transistor Q1 a constant load. The rectified and amplified signal is feed to the last transistor, Q4, an and-circuit, were also a strobe pulse discriminates a “1” “from a “0”. The short strobe pulse, 0,4 microsec., is initiated 0,8 microsec. after start of the read pulse. This timing has been determined according to measurements from reference 2. Actual read and write exercises of the final memory system has also proved this timing to be correct. The “1” is then transferred to the following register, the instruction memory register IMR. The read amplifier circuit has been long time-tested with a ±10% variation of voltage, different 2N393 with amplification from 39 to 400 and at a temperature range of –60 to +65°C before approval for satisfactory function.

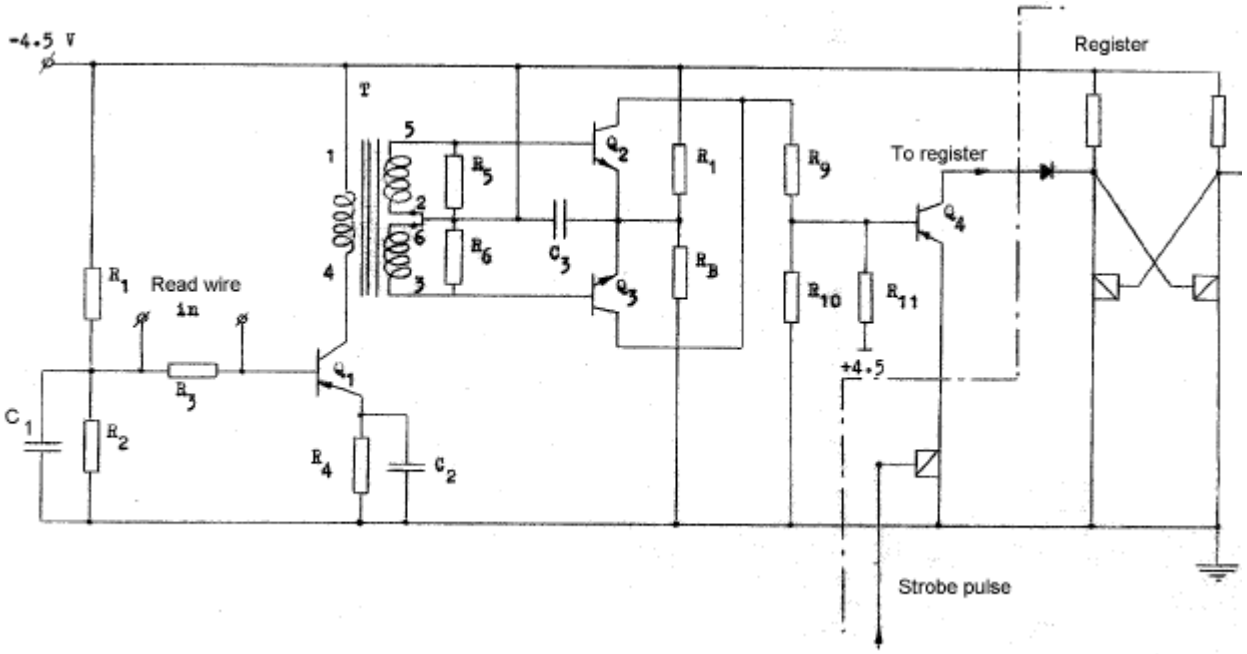


Figure 10. The read amplifier circuit with part of the following memory register.

An actual circuit board of the computer with three read amplifiers and inhibit circuits is shown in figure 12. Notice the three black 1:1:1 transformers and the heat sink which hides the driving power transistors Q5.

7. Inhibit driving circuit

The function of this circuit is to generate an inhibit pulse of about 200 mA, somewhat longer than the write pulse, when a “0” has to be written into a core. Information from the instruction register, IMR, together with an inhibit pulse initiates and amplifies so to drive the two parallel transistors, Q5 2N358 (ref. 6), each generating about 100 mA, figure 11. The power dissipation of the transistors is about the same as for the end transistors in the driving circuits. Elevated temperature affects the length of the pulse. About 15% of the 2N358 have been selected to keep the pulse length variation within 15 modules. Measuring resistors of 5 ohm are used when the driving pulses shape (read, write, inhibit) has to be studied.

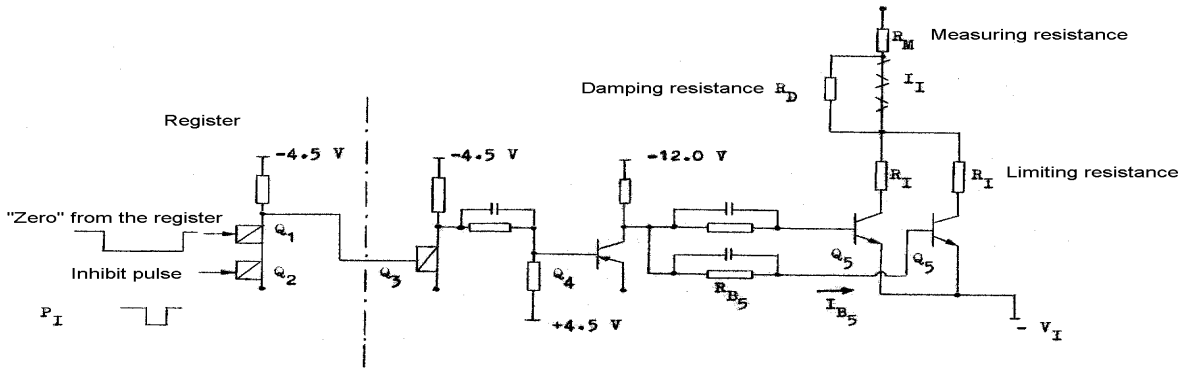


Figure 11. The inhibit driving circuit with input from the instruction register.

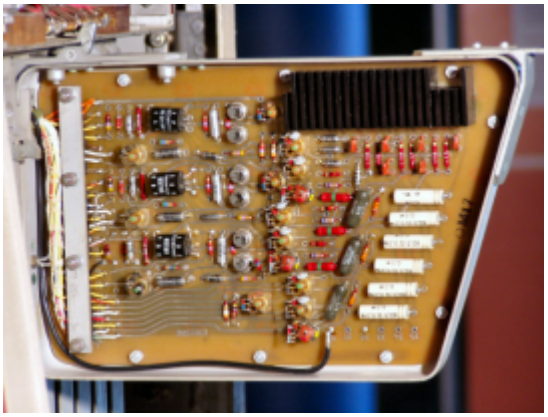


Figure 12. Photo of circuit board with read- and inhibit circuits

8. Other circuits

The address, instruction and memory register, with pure logic functions, are designed with “the unit circuit”. This contains a transistor, 2N393 (ref. 6), a capacitor, and two resistors (ref. 1, page 32). The same transistor circuit is used in the memory control unit that generates the read, write, and inhibit, address and strobe pulses. The “unit circuits” were designed with respect to variation of component parameters, temperature and 10% of supply voltage. It was necessary to consider the reaction and delay time of a chain of circuits in combination with the clock pulses. All circuits work synchronous, directed by the computer main clock pulse generator.

9. The mechanical design

All circuits are arranged on a number of two-layered printed circuit boards grouped around the memory packet M to get a short and compact arrangement. Wires for the driving current pulses are short and thick. The memory packet with all cards and the interconnecting wiring are housed in a supporting metal frame. The boards are all soldered o the interconnecting wiring to avoid influence from bad contacts. All boards can be turned out to make each component accessible for test or maintenance on both sides of the board. This arrangement fulfilled all test requirements during the run-in and operating period. Circuits with read amplifiers are placed close to the matrix package in order to get short length of read wires from package to amplifiers. Figure 13 shows the mechanical arrangement with the two memories on both sides of the control panels. Each memory system has the ferrite core packet in the middle (enclosed of a µ-metal screen) with the circuit boards above and below.

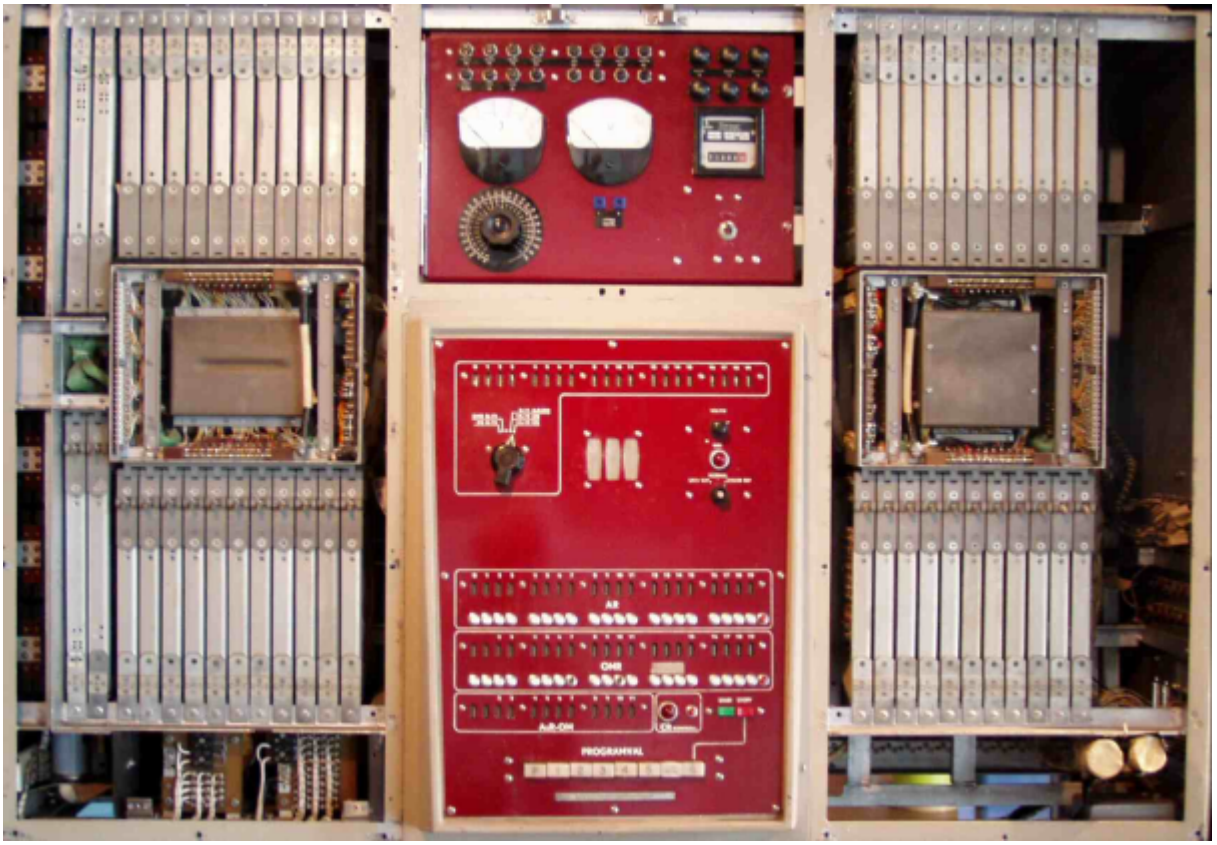


Figure 13. Arrangement of the circuit boards (folded back) around the memory packet in SANK-1. Variable data memory to the left and instruction to the right. The computer control panel in the middle at the bottom, supply regulation above.

10. Power supply

Circuits for logical operations use the transistor 2N393, “the unit circuit”, need ± 4,5 volt. Address and inhibit circuits use a –12 volt supply. A more complex system is used for feeding the read and write driving circuits. This system, ±11 volt, must also be variable with the temperature of the ferrite cores. This voltage is constant around room temperature operation. It is automatically varied from a temperature sensor in the memory package if temperature differs from room temperature.

It is necessary that the cores do not accidentally change information at power off, and that the program can start again just were it stopped. A special circuit senses when input power supply drops below a certain limit. This initiates a signal that the ongoing memory cycle is completed before a definitive stop of the memory functions is affected. Circuits that handle this function will deliver the blocking signal to transistor Tr5 in figure 5. The power supplies can deliver full power during this short time, about 6 microsec, after a power break. Power on is also sensed and the driving circuits of the memory will not be functional, until all voltages have reached their nominal values and the blocking signal ends.

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